REMARKS

Claims 1-13, 15-27, and 29-41 are pending, with claims 1, 15, and 29 being independent.

Claims 1, 9-13, 15, 23-27, 29, and 37-41 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Weng et al. (U.S. Patent No. 6,199,088). Applicants have amended independent claims 1, 15, and 29 to obviate this rejection.

As amended, independent claim 1 recites a multiply unit that includes, among other features, an arithmetic multiplier, a binary polynomial multiplier, permutation logic, and a multiply unit output data path. The multiply unit output data path includes one or more components to separately select the output of the arithmetic multiplier, the output of the binary polynomial multiplier or the output of the permutation logic to form a result.

As set forth in the application at, for example, Fig. 4 and page 12, lines 25-28, one or more multiplexers may be used to select the output of Marray 4100, MParray 4200, or permutation logic 4300 to form ResultC 3035. Applicants respectfully request reconsideration and withdrawal of this rejection because Weng fails to describe or suggest at least a multiply unit output data path that includes one or more components to separately select the output of the arithmetic multiplier, the output of the binary polynomial multiplier or the output of the permutation logic to form a result.

Instead, Weng discloses a circuit for performing a Galois Field division of two elements. The circuit includes a self multiplier 12, an element lookup table 14, a half multiplier, a permutation circuit, and a multiplier. See Weng, Fig. 2. The output of the self-multiplier 12 is used as the input to the element lookup table 14, the output of the element lookup table 14 is used as one input to the half multiplier, the output of the permutation circuit is used as a second input to the half multiplier, and the output of the half multiplier is used as an input to the multiplier. Using the output of the half multiplier, which computes A^{-1} using the outputs of the other components, and the input B, the multiplier produces the product $B * A^{-1}$, the sole output of the circuit. Thus, in Weng, the outputs of the self multiplier 12, the element lookup table 14, the half multiplier, and the permutation circuit cannot be selected. Rather, those outputs are used as

inputs for other operations and the result of the multiplier is the only possible output of the circuit.

For at least this reason, applicants respectfully request reconsideration and withdrawal of the § 102(e) rejection of amended independent claim 1 and its dependent claims 9-13.

Like amended independent claim 1, each of amended independent claims 15 and 29 recites an arrangement that includes a multiply unit output data path that includes one or more components to separately select the output of the arithmetic multiplier, the output of the binary polynomial multiplier or the output of the permutation logic to form a result. Accordingly, applicants respectfully request reconsideration and withdrawal of the § 102(e) rejection of amended independent claims 15 and 29, and their respective dependent claims 23-27 and 37-41, for at least the reason discussed above with respect to claim 1.

Claims 2-6, 16-20, and 30-34, which depend from claims 1, 15, and 29, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Weng in view of Bhandal (U.S. Patent No. 6,711,602). Applicants respectfully request reconsideration and withdrawal of this rejection because Bhandal does not remedy the failure of Weng to describe or suggest the features of claims 1, 15, and 29, as discussed above.

Claims 7, 8, 21, 22, 35, and 36, which variously depend from claims 1, 15, and 29, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Weng in view of Magar (U.S. Patent No. 4,538,239). Applicants respectfully request reconsideration and withdrawal of this rejection because Weng fails to describe or suggest the features of claims 1, 15, and 29, and Magar fails to remedy the deficiencies of Weng discussed above.

Applicants submit that all claims are in condition for allowance.

Enclosed is a $120.00 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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Joseph F. Key
Reg. No. 44,827

Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331

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